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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,333	12/31/2003	Toshiaki Kirihata	0928.0068C	9607

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EXAMINER	
SCHLIE, PAUL W	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 04/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,333	KIRIHATA ET AL.	
	Examiner	Art Unit	
	Paul W. Schlie	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-9,13-15 and 21-31* is/are pending in the application.

4a) Of the above claim(s) *2,4,10-12,16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-9,13-15 and 21-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3, 5-9, 13-15 and 21-31 have been examined as amended, with claims 2, 4, 10-12, and 16-20 being withdrawn, and claims 21-31 being new.

Response to Arguments

2. Applicant's arguments filed 3/27/06, with respect to the rejection of the original claims 2-3, 6-7, 16 and 18 under 35 U.S.C. 112 first paragraph have been fully considered and are persuasive; and have been correspondingly withdrawn in agreement that the means by which a memory core may be supplied with various voltages and/or sense amp circuitry may be constructed utilizing differing supply voltage rails which may thereby correspondingly affect said memory core's performance, is understood by those of ordinary skill in the art and thereby sufficiently enabled.

However the rejection of original claims 10-14 (now similarly embodied within amended claims 13-14, 21 and 28) under 35 U.S.C. 112 first paragraph is sustained, as they implicitly rely on the use of a common shared signaling medium as disclosed and conventionally utilized to interconnect elements within an integrated circuit, and which is conventionally understood as not being capable of supporting the simultaneous transmission of dissimilar data.

3. Applicant's arguments filed 3/27/06, with respect to the rejection of the original claims 1-20 under 35 U.S.C. 112 second paragraph have been fully considered and are persuasive; and have been correspondingly withdrawn in view of the applicant's correspondingly amended claims.

4. Applicant's arguments filed 3/27/06 with respect to the rejection of the original claims 1-20 (now 1, 3, 5-9, 13-15 and 21-31 as amended) under 35 U.S.C. 102(a)/103 have been fully considered but they are not persuasive. As per claims 1, 3, 5-9, 13-15 and 21-31 as amended, as Benini et al. is considered to teach that such a memory system as claimed may be automatically synthesized from an arbitrarily collection of memory elements which may themselves be constructed utilizing any commonly understood organization, circuit, and/or voltage generation techniques thereby inherently have differing attributes (inclusive of their inherent access, cycle, refresh cycles times and/or current/power consumption) as understood by one of ordinary skill in the art, and utilized by the synthesis process to guide their respective parametric selection based upon the said attributes as determined to be required based their respective placement or visa versa, as determined to be required to satisfy the logical and timing constraints defined by the description of the system which they may be selected and placed to compose. Thereby their rejection is sustained, and the rejection correspondingly clarified.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 13-14, 21 and 28 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure that is not enabling. Elements critical or essential to the practice

of the invention, but not included in the claims are not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

As per claims 13-14, 21 and 28, which seem related to the disclosed means by which memories which have different access times upon receiving a simultaneous access request may somehow simultaneously drive data onto a common signal line such that the two memory responses may be distinctly resolved, however not disclosed and considered a critical element not likely capable of being implemented by one of ordinary skill in the art at the time of the disclosed invention without undue experimentation; therefore not considered enabled.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 28 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. As the claim 15 from which claim 28 indirectly depends, cites that data received from said first and second memory arrays are received at about the same time, yet claim 28 cites reading said data sequentially within the implied context that the data is meant to be time/space division multiplexed to a common transmission medium (as rejected separately above), and is thereby is considered indefinite.

Corrective action is required, however new matter not supported by the original disclosure may not be added.

Claim Rejections - 35 USC § 102/103

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1, 3, 5-9, 13-15 and 21-31 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Benini et al. ("From Architecture to Layout: Partitioned Memory Synthesis for Embedded Systems-on-Chip", June 2001 DAC).

As per independent claims 1, 8 and 15, Benini et al. teaches that a memory system may be automatically synthesized which may contain multiple memory arrays which may be compose blocks of a larger logical memory, where each of which may correspondingly have a variety of differing properties either by original constraint, and/or as a result of the synthesis/selection/optimization process, including but not limited to: column/row organization, timing/performance, and power; based upon the temporal (i.e. frequency, performance and/or power goals), functional (i.e. volatile/non-volatile), and/or physical constraints (i.e. area, supply voltage, drive strength, impedance, placement, etc.); where their subcomponents, such as decode/control, and/or sense/driver

elements, may correspondingly have differing properties in attempt to optimize the physical design in accordance with the aforementioned synthesis constraints and/or goals (see sections 3.1, 3.2, 3.3, 3.4; and although not cited as the basis of this rejection US Patent 6,324,678 also reviewing logical/physical system synthesis). Thereby it is considered inherent that any memory implementation as resulting from such a synthesis process may comprise all the limitations claimed.

As per claims 3, 5-7, 9, 22-27 and 29-31, being dependant on claim 1, 8 15, or correspondingly dependant claim inclusively; in view that it is considered obvious to one of ordinary skill in the art that performance of memories are typically sensitive to supply voltage and/or organization (as reviewed above), and as such memories may thereby inherently comprise elements available to the synthesis process taught by Benini et al. and thereby inherently potentially parametrically selected based the performance requirement dictated by their placement (i.e. potentially selecting a slower lower voltage memory, different organization such as one having fewer cells per bit line, or differing sense amp architectures such as one biased to VDD, etc.; when in closer proximity to a memory controller than a correspondingly coupled memory placed further away); the claims are correspondingly rejected.

As per claims 13-14, 21 and 28, being dependant on claim 7, 8, 15 or correspondingly dependant claim inclusively, in view that it is considered obvious to one of ordinary skill in the art at the time of the disclosed invention that memory accesses and/or responses may be interleaved to improve data transfer bandwidth utilizing multiple memory banks (although not typically utilizing a common transmission medium

to support the simultaneous transmission of dissimilar data as implied in the disclosure, and thereby correspondingly rejected above), the claims are rejected.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul W. Schlie whose telephone number is 571-272-6765. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PIERRE BATAILLE
PRIMARY EXAMINER
4/7/06